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Effect of annealing on surface states of silicon gate capacitors.

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EFFECT OF ANNEALING ON SURFACE STATES OF SILICON GATE CAPACITORS

by

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ABSTRACT

In the fabrication of metal-oxide-semiconductor devices, the occurance of surface states has a significant influence on the final electrical characteristics. To insure a reliable and reproducible process, the factors effecting the magnitude of the states are investigated. The analysis is performed on test capacitors fabricated according to the basic process steps of the Silicon Gate technology modified to accomodate the titanium. paladium, gold interconnecting metallization. Combinations of times from five minutes to four hours, ambients of 10% hydrogen to 100% hydrogen, and temperatures from 400°C to 800°C are used to determine the critical annealing parameters.

With a sufficient hydrogen atmosphere, a steady state value of N_{ss} with time is obtained regardless of other parameter variations. This makes time the major variable with temperature and ambients having secondary effects. A number of time constants are associated with the variations of the process. For a particular set of parameters the time constants are compared with the theoretical diffusion times, proving that the annealing process is not diffusion limited. The annealed affects are associated with the phenomena occuring at the silicon-

oxide interface.

A hydrogen ambient threshold is determined to exist between 10% and 50% hydrogen in nitrogen. Below this threshold the effects of the parameters behave differently. The 10% hydrogen is inadequate in terms of final N_{ss} values to properly anneal surface states. There also exists an optimum temperature range above and below which the fast state values increase. This reinforces Kooi's model of the unstable Si-H bonds and accentuates the results of Castro and Deal.

The effects of increasing the quantity of hydrogen constituents with increasing temperature is verified by a decrease in the N_{ss} values for the 5 minute anneal. This decrease is predicted by the equation for free-energy change. For times greater than 5 minutes, the unstable Si-H bonds and an excess of hydrogen molecules dilute the results predicted by this equation.

1. Introduction

Surface states, also called fast states, exist at the interface of the silicon substrate and oxide layer. They are a result of disturbances in the periodic crystalline lattice structure and can number between $10^{14}/cm^2$ for freshly cleaved silicon surfaces to $10^{10}/cm^2$ for carefully prepared passivated samples. If a potential is applied to the silicon surface, the energy states move with the valence and conduction energy bands. When the surface states pass through the fixed fermi level an exchange of charge occurs. This results in a change of the voltage drop across the oxide, and a distortion of the capacitance-voltage curves as shown in figure 1.[1] The voltage drop due to the surface state charge Q_{ss} and the silicon depletion layer charge Q_D is:[2]

$$V = - \frac{Q_{ss} + Q_D}{C} \qquad (1)$$

C is the gate to channel capacitance per unit area (F/cm^2). Besides distorting the voltage drop across the oxide and silicon, the measured device capacitance, C_m, is also affected. The surface state capacitance, C_{ss} in figure 2, is parallel to C_D, the silicon depletion layer capacitance and in series with the oxide capacitance, C_{ox}. The resulting measured capacitance increases with the existence of fast

states. The surface state resistance and capacitance elements of figure 2 vary with bias voltage. Their distribution is usually not uniform across the energy gap.

Balk[3] demonstrates that the fast states per square centimeter, N_{ss}, are significantly reduced by applying an aluminum layer over the oxidized slice and heat treating in a nitrogen atmosphere at 500°C. This process is called "alneal." Subsequent studies reinforce Balk's original theory that during the alneal some species of hydrogen are responsible for the reduction of fast states.

Silicon Gate technology is important in the manufacture of MOS circuits, especially Random Access Memories. The test vehicle used in this thesis parallels this technology, using titanium, paladium, and gold to contact the many individual electrical devices. The absence of aluminum requires the use of hydrogen gas annealing in place of the alneal process. Little information exists describing the effects of time, temperature, and annealing ambient on the N_{ss} results of this structure.

The Quasi-Static Capacitance-Voltage measurement is used in Section 2.2 to evaluate the fast states around midgap, 0.5 ev above the valence band. The results are useful in understanding the mechanism of the annealing process.

2. Measurement of Surface States

2.1 Evaluation Methods

A number of methods are available to evaluate the

surface states of a MOS structure. The most important are reviewed here.

A high frequency capacitance technique is proposed by Terman.[4] It involves measuring the capacitance voltage curve and comparing it to the theoretical one. A graphical differentiation is required to determine a surface state distribution. Also, the surface state charging time must be larger than the period of the testing frequency.

Goetzberger and Nicollian[5] perfected a conductance technique. It is the most detailed and accurate method to produce the MOS admittance as a function of bias and frequency. It has the disadvantage of requiring a large number of measurements to obtain the surface state distribution between midgap and the fermi level. This limited energy range requires both "n" and "p" types of material to observe the distribution in a large part of the band gap.

The Gray-Brown technique[6] shows the surface state density near the majority carrier band edge. It requires measuring the MOS capacitance with respect to temperature gradients. The method is limited at high temperatures by the oxide instability and at low temperatures by the ionization of impurities. One disadvantage is the small area of the analyzed band gap.

A low frequency method of measuring surface states, conceived by Berglund,[7] maintains thermal equilibrium of the test device. The surface state distribution is obtained

over a large portion of the band gap. A major disadvantage is in the physical measurement below five hertz where Berglund found Capacitance-Voltage dispersion.

The use of a Quasi-Static capacitance voltage measurement is reported by Kuhn in 1969.[8] He obtains low frequency measurements of a MOS capacitor using a linear voltage ramp. The surface potential is measured, allowing for the determination of the surface state distribution over a large part of the energy gap without graphical differentiation. Also, the possibility of combining high frequency and quasi-static curves to obtain fast state densities at mid-gap with an accuracy of $\pm$ 10 $^{10}/_{cm^2}$ [9] is especially attractive for analysis of large amounts of data. Therefore, the quasi-static measurement technique is selected as most suitable for our analysis.

2.2 Quasi-Static Method

The Quasi-Static technique requires the measurement of the MOS displacement current in response to a linear voltage ramp as described in figure 3. The displacement current

$$i(v) = C(v) \frac{dv}{dt} \qquad (2)$$

is a function of the MOS capacitance, C(v), and the voltage sweep rate, dv/dt, of the ramp generator. The capacitance

at any applied voltage can be determined if the displacement current, measured by an electrometer and the sweep rate are known.

If an input voltage, $V_{in}(t)$, is applied to the circuit of figure 3, then the output voltage, $V_o(t)$, is

$$V_o(t) = C(v) \frac{d\, V_{in}\,(t)}{dt} \tag{3}$$

If the input voltage is a ramp function described by

$$V_{in}\,(t) = V_1 \pm \alpha t, \tag{4}$$

where V_1 is a DC component and α is a constant, the output voltage as a function of time is

$$V_o\,(t) = \pm \alpha RC\,(t) \tag{5}$$

It depends on the differential capacitance. Therefore, the output voltage, $V_o\,(t)$, corresponds directly to a plot of C (v) versus V.

The surface state distribution as a function of surface potential, $N_{ss}\,(\psi s)$, is related to the surface state capacitance, C_{ss}, a function of surface potential, and to the elementary charge, q. $N_{ss}\,(\psi s)$ is given by

$$N_{ss}(\psi s) = \frac{C_{ss}(\psi s)}{q} = \frac{1}{q}\left[\frac{C(Va)}{1-\frac{C(Va)}{C_{ox}}} - C_{ss}(\psi s)\right] \quad (6)$$

C(Va) is the measured MOS capacitance obtained from

$$1/C(Va) = 1/C_{ox} + 1/[C_{sc} + C_{ss}] \quad (7)$$

C_{ox} the oxide capacitance, farads per unit area, C_{sc} the ideal low frequency semiconductor capacitance. To validate equation (6), the thermal generation rate must be larger than the applied sweep rate. R. Castagnē[10] demonstrates that over a limited energy range, from accumulation to the onset of inversion (surface potential = 2 x fermi energy), the high frequency and quasi-static capacitance voltage curves are utilized to directly yield the surface states. The dispersion of the curves is related to the fast state distribution:

$$N_{ss} = \frac{C_{ss}}{q} = \frac{1}{qA}\left[\frac{C_{lf}C_{ox}}{C_{ox}-C_{lf}} - \frac{C_{hf}C_{ox}}{C_{ox}-C_{hf}}\right] \quad (8)$$

C_{lf} and C_{hf} are the low frequency and high frequency capacitances respectivly at an applied voltage V_a, A the capacitor area, and C_{ox} the oxide capacitance. This expression does not require a knowledge of surface potential and is ideally suited for the proposed work at midgap where it is the most accurate.

Berglund[7] first suggested obtaining the surface

potential from low frequency capacitance-voltage curves in thermal equilibrium. The low frequency (quasi-static) capacitance curve is integrated from strong accumulation, V_{acc}, to strong inversion, V_{inv},

$$\psi(V_a) = \int_{V_{acc}}^{V_{inv}} \left[1 - \frac{C(V_a)}{C_{ox}}\right] dV_a + \Delta \qquad (9)$$

Eq. 9 yields the surface potential as a function of applied voltage to within one additive constant, Δ, that is obtained by first evaluating the integral in equation (9). Its difference from the known band gap of 1.1 ev is divided then by 2, and the resulting value added to the surface potential, thus centering the measured range in the band gap.

2.3 Testing Procedures

The arrangement of the equipment for monitoring fast states is shown in figure 4. The capacitance is measured by a Booton model 71A-R capacitance-inductance meter. The test signal frequency is 1 MHZ, its level fixed at 15 mv rms. The ramp voltage is supplied by a Hewlett Packard, Model 3310 B generator operating in the continuous mode. Sweep voltage is $\pm$ 5.0v about a zero center point. Sweep rates are capable of less than 5 millivolts per second to 50 v/sec. The operational amplifier measuring the displacement current is a Keithley 610 C electrometer, operating in fast mode. Rigid shielding between probe contact

and input of the electrometer reduced the spurious noise interfering with the measured curves. The probe point is made of tungsten carbide, the wafers are mounted on a vacuum-thermal chuck and the x-y recorder is a Hewlett-Packard 135 AM.

Several tests were conducted. To assure a minimum contact resistance between the back of the test chip and the vacuum chuck, the device was biased into strong accumulation to obtain the oxide capacitance. If the contact is poor, the measured oxide capacitance is significantly less than the theoretical capacitance

$$C_{cal} = \frac{K\epsilon_o d}{A} \qquad (10)$$

K is the dielectric constant and ϵ_o is the permittivity of free space equal to 8.86×10^{-14} F/cm. The thickness of the oxide, d = 1150A, is obtained using a Perkin-Elmer ellipsometer. A is the field plate area.

The theoretical capacitance is 460 pf and the measured capacitance 450 pf. These values deviate only 2% from one another verifying good ohmic contact.

Nonequilibrium conditions can be present during low frequency capacitance voltage measurements. Kuhn and Nicollian[11] discuss the effect of slice illumination under test, an excessive sweep rate, and a long silicon time constant. The deviations result in a voltage shift and a peak

near weak inversion when sweeping from inversion toward accumulation, or deep depletion when sweeping from accumulation toward inversion. These effects are explained by field induced junctions and must be minimized to obtain accurate data. Therefore, the test devices are probed in a light tight box surrounding probe and vacuum pedestal. The sweep rate is reduced to 5 millivolts per second, but this is not sufficient to rid the curves of distortion caused by silicon time constants greater than 100 microseconds. To obtain ideal curves, the devices are heated to 80 $\pm$ 1°C. This increases the thermal generation rate over the displacement current as described by Kuhn and Nicollian. With the heating of the substrate, the sweep rate is increased to 25 millivolts per second. Some distortion is observed when the sweep is increased to 50 millivolts per second.

3. Preparation

3.1 Test Vehicle

To evaluate the effects of annealing on silicon gate technology, test capacitors are fabricated in the following manner. A single crystal, Czochralski grown silicon substrate, <111> orientation, is phosphorus doped to produce an "n" impurity level of approximately $10^{15}/cm^3$. Over this substrate a thermal "gate oxide" is grown to a thickness of 1250 $\pm$ 50 A° measured with a Perkin-Elmer ellipsometer. The oxide is then etched to 1150 $\pm$ 50 A° immediately prior to the deposition of the field plate, consisting of a "p"

dopant. Finally, phosphorus pyrolytic oxide is deposited over the entire slice to insure ionic stability, and a window is cut through this oxide for contacting the field plate. Temperature-bias, drift-studies were made on two slices from each group of test vehicles. The temperature was $200^{\circ}C$, the bias $2x10^{6}$ volts per centimeter, and the time at temperature and bias was one hour. Twenty wafers representing the test group did not experience a flatband voltage drift from before to after test exceeding .08 volts. This demonstrates excellent stability. After a window was cut into the oxide for access of the field plate, the annealing experiments are performed. Good ohmic contact was assured by evaporating paladium on the field plate and sintering in an inert ambient, thus forming low resistive paladium silicide. Figure 5 shows a cross sectional view of the resulting capacitor. To insure good electrical contact between test chuck and substrate, a layer of aluminum, approximately 1000Å thick, was evaporated on the underside of the test chip. The field plate of the capacitor is $1.73x10^{-2}$ cm^{2}. Two advantages result from using a capacitor of this small size. (1) The displacement current is in the range of 10^{-9} amperes, that is four orders of magnitude larger than the noise currents inherent in the test system. (2) The number of oxide defects per capacitor is reduced, thus avoiding premature voltage breakdown that would limit the availability of test devices.

3.2 Experimental Anneal Parameters

To evaluate the contributions of various annealing parameters, a group of test devices have the annealing step omitted from the capacitor processing. The fast states of these devices represent the process up to the annealing step. They are compared to the fast states of those devices that underwent the annealing treatment.

The effect of time at elevated temperature and ambient is investigated. Annealing times range from five minutes to four hours. From the curves of N_{ss} versus time, the activation energy of the hydrogen through the dual layer polycrystalline silicon-oxide structure is obtained. The activation energy is then used to evaluate diffusion coefficients, establishing whether or not annealing of fast states is diffusion limited. Also from the curves, an optimum annealing time is established indicating to what extent time is a factor in annealing operations.

As stated by Castro and Deal,[12] Montello and Balk,[13] and theorized by Kooi,[16] an optimum annealing temperature is expected. Temperatures investigated usually range from 400°C to 600°C, sometimes also higher temperatures were applied.

Finally, the reduction effect of hydrogen in the annealing ambient was investigated. It was theorized[14] that ionic or atomic species of hydrogen are responsible for the annealing phenomenon. The amounts of hydrogen released

under various conditions fluctuates and the decrease in the content of hydrogen is expected to show a similar increase of fast states. To substantuate this theory, three ambients are used for annealing, 10% and 50% hydrogen in a nitrogen ambient, and 100% hydrogen. Pure nitrogen was not used because of significant studies already performed.[12] The alterations of all the variables investigated here are shown in table I.

3.3 Annealing Procedure and Equipment

The annealing step is performed in a resistance heated furnace capable of controlling the experimental zone temperature to $\pm$ 1/2°C. A Quartz tube is inserted into the furnace with one end necked to accept fittings for the appropriate gases, the other end is open to accept the experimental devices. After the wafers are inserted into the furnace, an end cap made of stainless steel fits over the end of the tube completely sealing the system. The wafers sit on a quartz boat with an attached quartz handle. The handle fits through a "Swage Lock" fitting in the end cap allowing the resealing of the system after the wafers are positioned in the furnace. About ten inches of the quartz tube at the end cap protrude from the furnace. This part of the tube reaches a temperature of 180°C. Temperatures in the hot zone are measured with a Platinum - Platinum 10% Rhodium thermocouple connected to a digital readout. The

temperature in the holding zone is monitored using an Iron-Constantan thermocouple, more appropriate for lower temperatures. The wafers, ready for a particular set of variables, hold in this end of the tube until it is flushed with nitrogen, expelling the oxygen and avoiding any mishaps that might occur with the gas mixture. The required hydrogen content is put into the tube and the wafers are inserted into the hot zone for the required annealing time. This method avoids the nitrogen purge problems that plagued Castro and Deal.[12] Each run received a five minute nitrogen pre-purge and a five minute nitrogen post-purge. The post-purge is done after the required annealing time has expired, and the wafers are pulled into the holding zone.

The furnace and gas delivery system is constructed according to figure 6. The mixture of gases, 10% or 50% of hydrogen in nitrogen according to volume is established using Brooks flow-rates model R-15-B for N_2 and R-2-15-B for hydrogen. Both nitrogen and hydrogen gases are obtained from liquid sources. The moisture in the furnace, always reading less than 3 parts per million, is monitored by a "Meeko" moisture analyzer attached to the working tube. The hydrogen flow is held at two liters per minute while the nitrogen is varied to give the required 10% or 50% mixtures. A pressure gauge is installed to check for possible gas leaks that occurred during the assembly of the system and also to monitor any back pressure of the gases.

4. Results and Proposed Models

4.1 Hydrogen Threshold

Figures 7 through 9 display N_{ss} as a function of annealing time for all ambients. Each figure is for a different annealing temperature. Although the N_{ss} values for the three ambients decrease with increasing annealing time, there are two separate and distinct trends. The N_{ss} values of the 50% and 100% hydrogen ambients have a singular steady state value. Considering N_{ss} differences due to flucuations in the processing and experimental error, the final values from 400°C to 600°C at the end of 4 hours differs by only $10^{10}/cm^2$. This small difference for two hydrogen ambients indicates that the annealing time is a dominate factor in the process. Given a sufficient initial hydrogen concentration, flucuations in hydrogen contents or annealing temperatures are insignificant. The achievement of one single N_{ss} value for the 50% and 100% hydrogen ambients does not apply to the 10% hydrogen atmosphere. After 4 hours of annealing, the resulting fast states are between $5x10^{10}$ to 10^{11} greater than for the 50% or 100% values. This difference between the two sets of curves indicates the existence of a hydrogen threshold between 10% and 50%. Below this value the fast states are not sufficiently annealed.

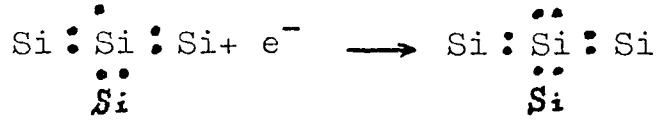
4.2 Optimum Annealing Temperature

In progressing from figure 7 to figure 9 the 10%

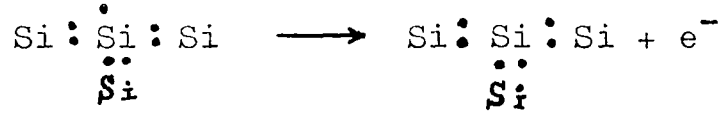
hydrogen curve for N_{ss} decreases at 500°C and then rises again for 600°C. Castro and Deal[12] reported an optimum annealing temperature somewhere in the range of 400°C to 500°C for ambients of 100% nitrogen and 50% hydrogen in nitrogen. Later they noticed that the increase in fast states with an increase in temperature was associated with the nitrogen purge that preceeded and followed each experimental run; the purge technique was modified in this work to avoid this influence. Their observation leads to the conclusion that an insufficient hydrogen atmosphere results in an optimum annealing temperature. Figure 10 is a plot of N_{ss} at midgap as a function of annealing times for various furnace temperatures using the 10% hydrogen ambient. 400°C is an undesirable temperature insufficiently annealing the surface states. The other three temperatures all seem to approach a steady state value at about the same rate. The outstanding result obtained from this figure occurs after four hours at temperature and ambient. The N_{ss} value decreases from the 400°C curve to the 500°C curve and then increases at 600°C. Finally, the N_{ss} value takes a large increasing step at 800°C.

An optimum annealing temperature indeed appears at sufficiently long annealing times for 10% hydrogen. Castro and Deal also observed that "shorter anneal times at a given temperature tend to give lower densities of fast states."[12] Considering that this statement was based on

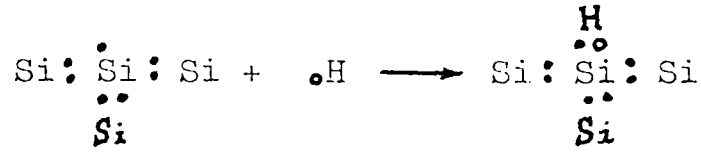
results adversly effected by the nitrogen purge, we can only substantiate their conclusion at 800°C between one hour and four hours where N_{ss} increases with time. The existence of an optimum annealing temperature can possibly be explained by the theory of unsaturated bonds proposed by Kooi.[16] A single unpaired electron of a silicon atom bonded to three other silicon atoms can be considered an acceptor



or the group of silicon atoms can be considered a donor by losing the unpaired election.



Due to a probable misfit or lack of oxygen atoms, not all the valences of the silicon groups are saturated. This gives rise to acceptor or donor states that communicate with the conduction or valence bands, respectively. During the heat treatment in hydrogen, the atom combines with a number of these acceptor or donor states eliminating their enhancing effects on N_{ss}



This basically explains the annealing of fast states in a hydrogen atmosphere. Low temperatures probably do not provide the energy necessary for formation of a sufficient number of bonds to anneal the surface states. Increasing the temperature produces an increasingly unstable Si-H bond that eventually disintegrates, increasing the N_{ss} values. As a result, both temperature extremes produce unsaturated silicon bonds that contribute to increased surface states, thus there is a compromise between these temperatures where the N_{ss} is minimal. This result only occurred for the 10% hydrogen ambient after a sufficient time interval, the behavior of 50% and 100% hydrogen atmospheres was different. The probability of producing unsaturated bonds in the presence of an extensive number of hydrogen atoms is smaller and the effects at high temperatures do not apply.

4.3 Time Constants

Figures 11 and 12 each display for a single ambient a decrease in N_{ss} as a function of time for different temperatures. These curves are approximated by a decreasing exponential function, each curve having its own time constant. The reduction in N_{ss} is possibly attributed to the chemical reaction occurring at the silicon oxide interface as theorized in section 4.2 or it may be the result of a limited hydrogen diffusion through the dual layer

polycrystalline silicon-silicon dioxide structure.

To establish the mechanism for the decrease in N_{ss}, time constants for each set of annealing variations are compared to theoretical diffusion times. The time constants of figures 11 and 12 were obtained by plotting these curves in a normalized form

$$\frac{N_{ssf}\ (t=\infty)}{N_{ss}(t)} = f(t) \tag{11}$$

in linear scale as shown in figure 13 for 400°C, 50% hydrogen. The measured points are approximated by

$$\frac{N_{ssf}}{N_{ss}(t)} = (1-e^{-t/\tau}) \tag{12}$$

t is the annealing time, τ is the time constant for the particular curve. A plot of t/τ as described by

$$t/\tau = \frac{N_{ss}(t)}{N_{ss}(t)-N_{ssf}} \tag{13}$$

and shown in figure 14 should produce a slope equal to $1/\tau$, the reciprocal of which will result in the time constant of 110 minutes. For the other annealing variations encompassing 400°C, 500°C, 600°C temperatures and 50%, 100% hydrogen ambients, the corresponding time constants are displayed in table II.

The time required for hydrogen to diffuse through

SiO_2 or Si can be approximated by[17]

$$d = 2\sqrt{Dt} \qquad (14)$$

d is the resulting depth in which hydrogen will diffuse in time t, D is the diffusivity constant equal to $3x10^2$ /hr.$^{1/2}$ for SiO_2 and 10^3 /hr.$^{1/2}$ for Si at 400°C. For an oxide thickness of 0.1 microns and a polysilicon thickness of 0.4 microns, the time required for the diffusion of hydrogen according to equation 14 is a few milliseconds. Since the measured time constants in table II are on the order of hours and the diffusion time is in fractions of seconds, the annealing results cannot be effected by a diffusion limited process. The measured time constants must be a result of the chemical reactions at the interface.

4.4 Effects of Hydrogen Constituents

Several papers argue[3,14,15] that species other than molecular hydrogen is responsible for the annealing of fast states. A number of reactions take place with the silicon gate structure that would liberate atomic or ionic hydrogen

$$H_2 \rightleftharpoons 2H \qquad (15a)$$

$$e^- + H \rightleftharpoons H^- \qquad (15b)$$

$$H \rightleftharpoons H^+ + e^- \qquad (15c)$$

$$2\ \text{Si (polycrystalline)} + H_2 \rightleftharpoons 2\ \text{Si H} \qquad (15d)$$

$$\text{Si H} \rightleftharpoons \text{Si} + \text{H} \qquad (15e)$$

In these reactions and in others capable of producing the required species of hydrogen, there is a free energy change, ΔF, associated with the reactions:[18]

$$\Delta F = -RT \ln K \qquad (16)$$

it depends upon a number of variables, R the universal gas constant, T the temperature, K the equilibrium constant of an ideal gas. For the case of molecular hydrogen, H_2, disassociating into atomic hydrogen, H, according to equation 15a

$$K = \frac{(H)^2}{(H_2)} \qquad (17)$$

$(H)^2$ and (H_2) are the constituent mole fractions of each species of hydrogen in the equilibrium gas mixture. H_2 equals 1 at one atmosphere. Solving for the atomic constituent using equations 16 and 17 results in

$$(H)^2 = H_2\ e^{-\Delta F/RT} \qquad (18)$$

The amount of atomic, or ionic hydrogen is directly

proportional to temperature. To substantiate this theory a decrease in N_{ss} as a function of temperature should be anticipated. Figures 15, 16, 17 are plots of N_{ss} as a function of temperature for various ambients, each graph is for a different annealing time. Figure 15 is the most supportive of this theory. For all three ambients at five minutes annealing time, the N_{ss} values decrease with increasing temperatures. Observing the final values at 600°C and comparing this spread in N_{ss} to that at 500°C indicates that the initial percentage of molecular hydrogen is still the most influential. Increasing the constituents with temperature is of secondary importance. For increased annealing times, figures 16 and 17 lose the definitiveness of figure 15. The 10% hydrogen curves of figure 16 and 17 show the influence of the unstable Si-H bond and the 50% and 100% hydrogen ambients are erratic in their N_{ss} changes. The 60 minute anneal time of figure 17 totally outshadows any effects of temperature and results in a zero slope.

For the short annealing time of 5 minutes, the results of increasing the temperature are most dramatic and support the theory of hydrogen species effecting the anneal. As the time is extended, the unstable Si-H bond in the case of 10% hydrogen and most probably an over abundance of hydrogen constituents in the case of 50% and 100% hydrogen ambients dissolve any effects of temperatures according to equation 23. This is apparent in figures 18, 19, and 20 where N_{ss}

is plotted, for various annealing times, each graph is a different ambient.

5. CONCLUSION

In order to properly anneal the fast states of the test capacitors, a minimum N_{ss} is desirable. The optimum annealing conditions should be insensitive to pertubations that normally accompany manufacturing processes.

Temperatures investigated indicate that above the hydrogen threshold, 400°C, 500°C, or 600°C all approach one single limiting value, not favoring any temperature.

To guard against the effects of contaminating the annealing gas and reducing the hydrogen content, an optimum annealing temperature of 500°C, obtained for low hydrogen content, should be selected.

The 10% hydrogen content is undesirable because it insufficiently anneals surface states. The selected ambient should have at least the minimum quantity of hydrogen corresponding to the hydrogen threshold. 50% and 100% hydrogen ambients show the same final annealing results. The gas mixtures above the threshold should then be chosen on the ease of use, i.e. 50% hydrogen or less for safety.

Annealing time, as major parameter is important. Having selected optimum temperature and ambient, the steady state value of N_{ss} is approached after at least 80 minutes of heat treatment. If the annealing time is increased to

100 minutes, little if any deviations in N_{ss} will result.

A viable and reproducible process for annealing of fast states with hydrogen gas is obtained. It requires a temperature of 500°C, ambient of 50% hydrogen in nitrogen, and a time of 100 minutes. This should reduce the final N_{ss} to the range of $2 \times 10^{10}/cm^2$ and fulfills the requirement of insensitivity to variations of processing.

TABLE I

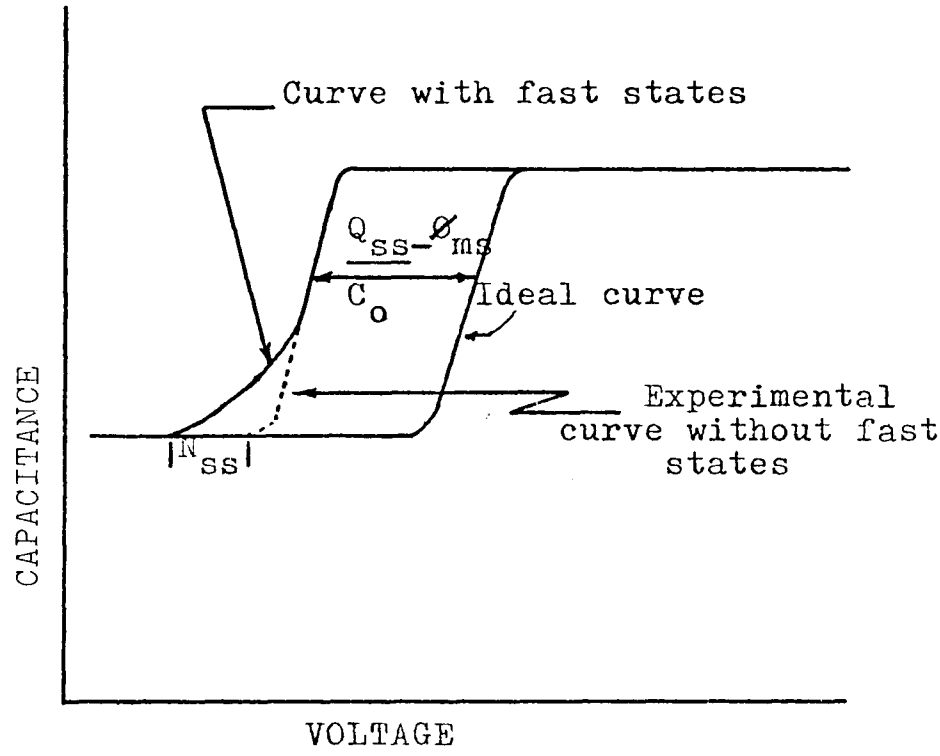
ANNEALING VARIATIONS

Annealing Temperature	Annealing Ambient		
	10% H_2	50% H_2	100% H_2
400°C	5 min.	5 min.	5 min.
	30 min.	30 min.	30 min.
	60 min.	60 min.	60 min.
	240 min.	240 min.	240 min.
500°C	5 min.	5 min.	5 min.
	30 min.	30 min.	30 min.
	60 min.	60 min.	60 min.
	240 min.	240 min.	240 min.
600°C	5 min.	5 min.	5 min.
	30 min.	30 min.	30 min.
	60 min.	60 min.	60 min.
	240 min.	240 min.	240 min.
800°C	5 min.		
	30 min.		
	60 min.		
	240 min.		

TABLE II

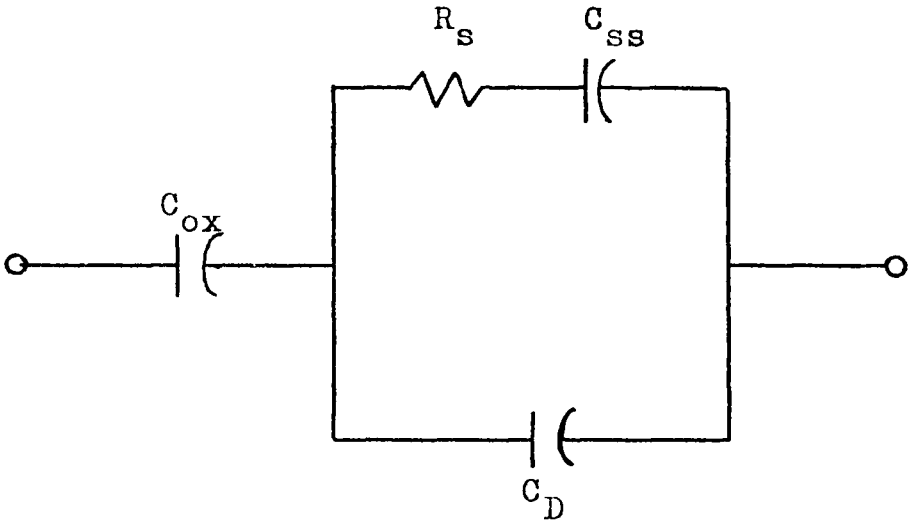
TIME CONSTANTS

<u>50% Hydrogen</u>	
400°C	= 111 minutes
500°C	= 42 minutes
600°C	= 25 minutes
<u>100% Hydrogen</u>	
400°C	46 minutes
500°C	40 minutes
600°C	10 minutes



Q_{ss} = surface state charge
C_o = oxide capacitance
N_{ss} = resulting fast states
ϕ_{ms} = metal-semiconductor work function

Figure 1. Capacitance Voltage Distortions



C_{ox} = Oxide Capacitance
C_D = Depletion Region Capacitance
R_s = Surface State Resistance
C_{ss} = Surface State Capacitance

Figure 2. Equivalent Circuit of Metal-Oxide-Semiconductor Capacitor

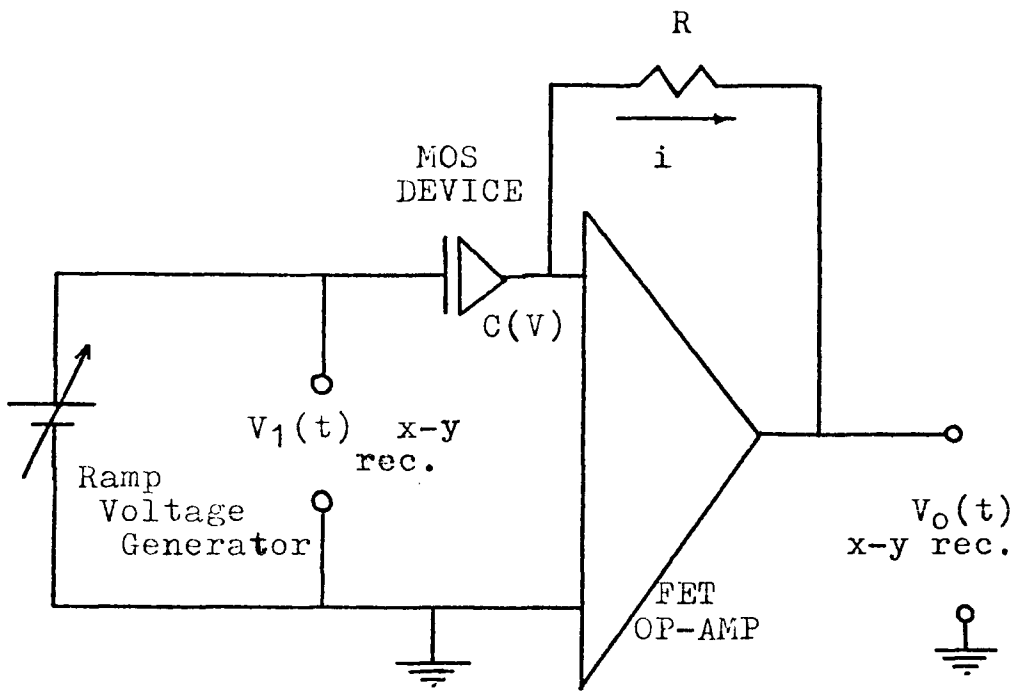
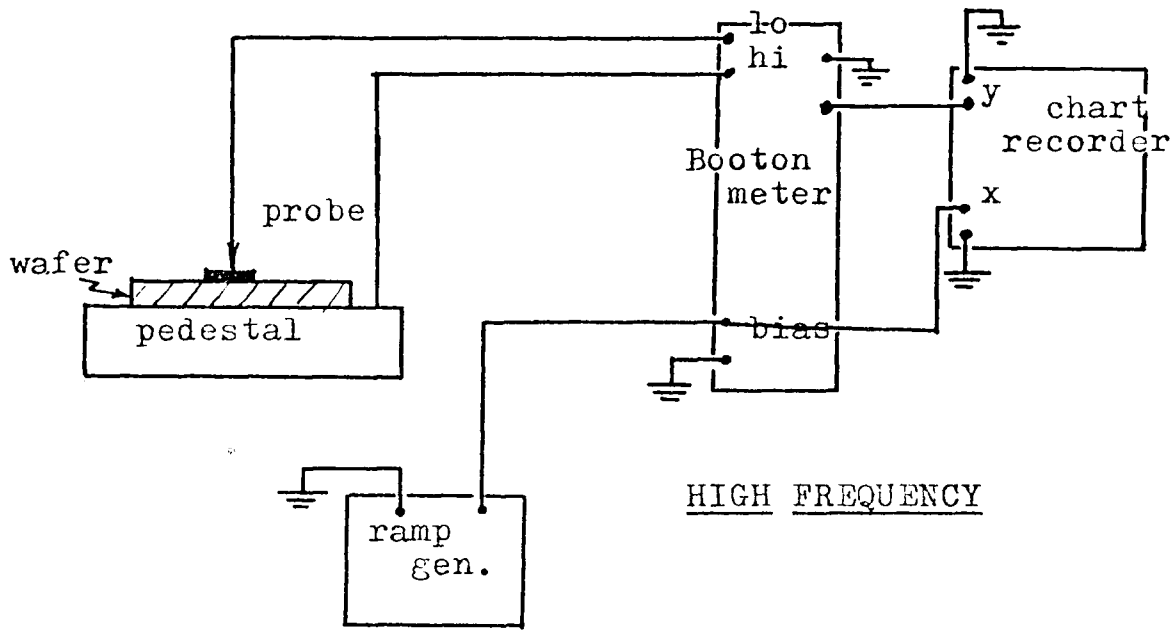


Figure 3. Circuit Requirements for Quasi-static Measurements



LOW FREQUENCY

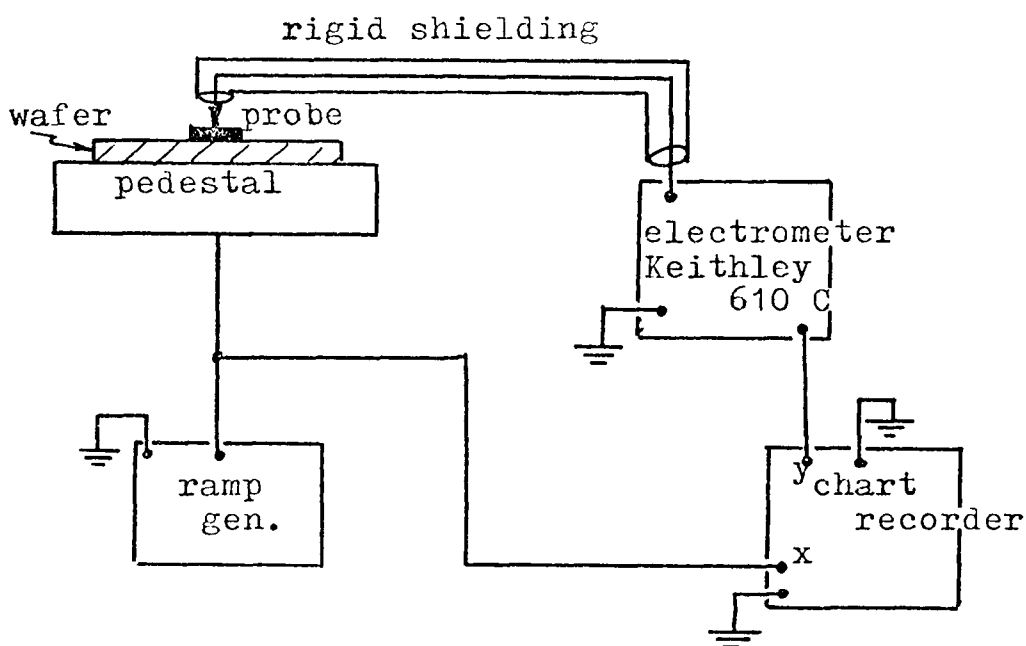


Figure 4. Equipment Arrangement for High-Low Frequency MOS Measurements

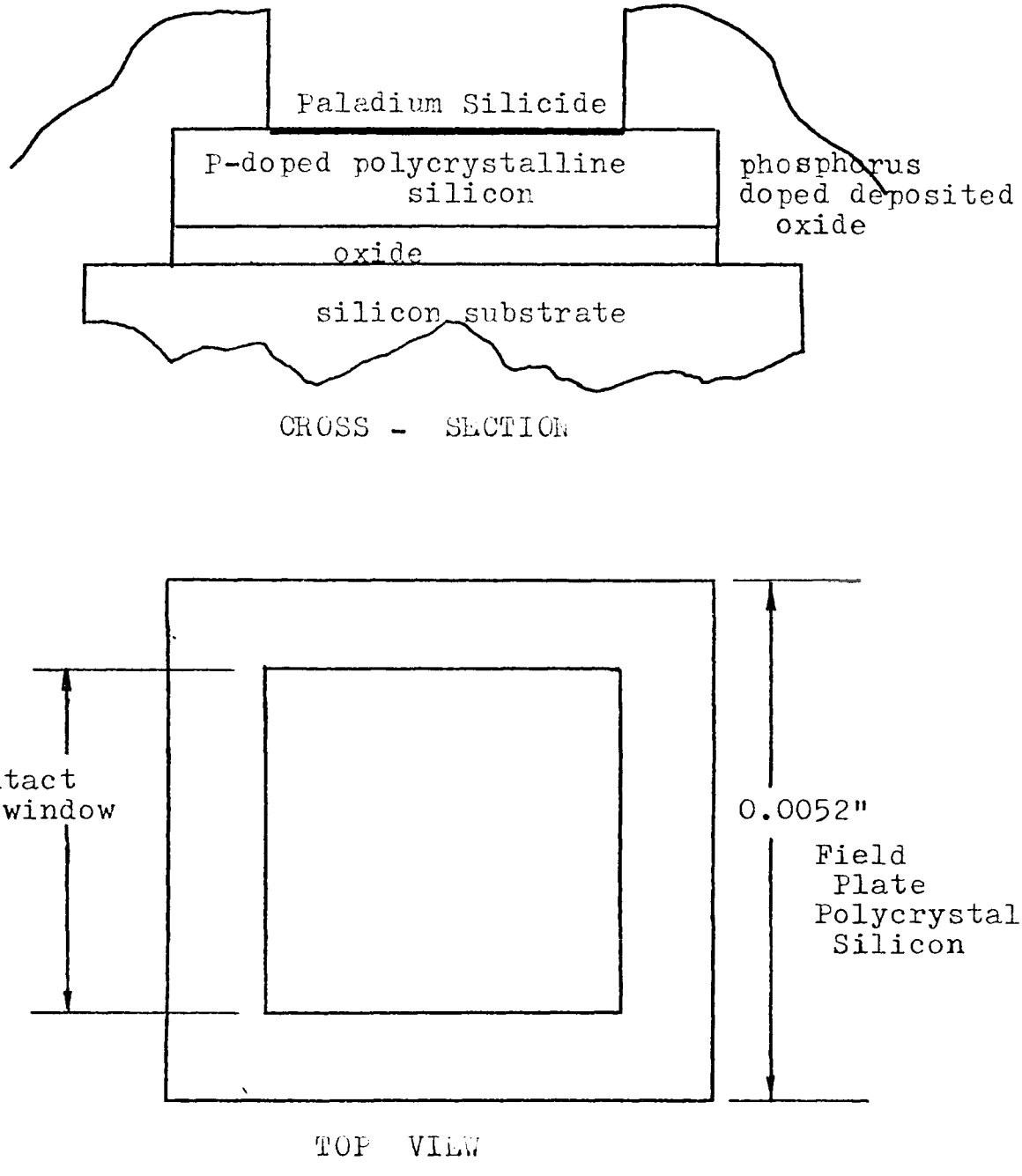


Figure 5. Structure of Test Capacitor

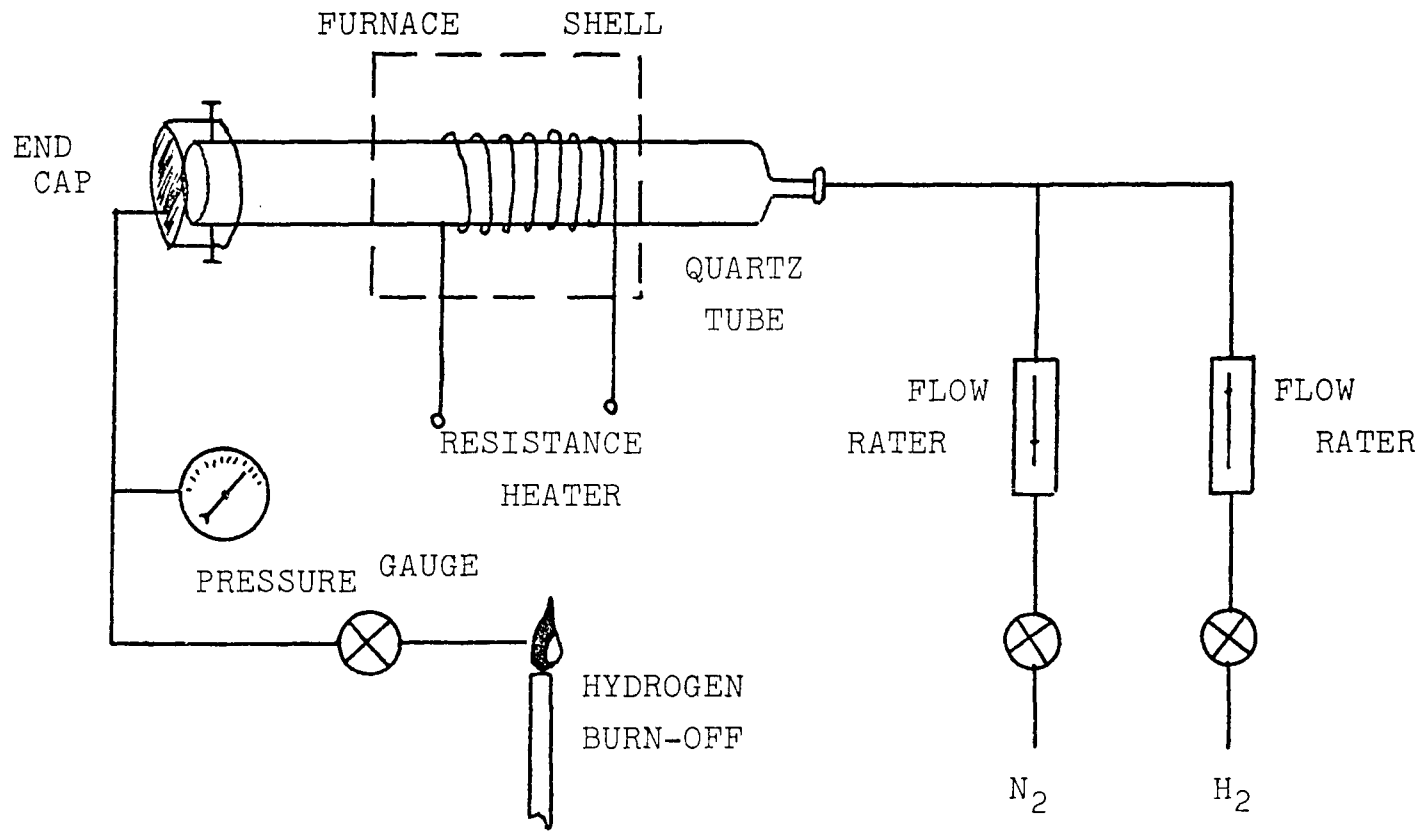


Figure 6. EQUIPMENT ARRANGEMENT FOR ANNEALING SILICON SLICES

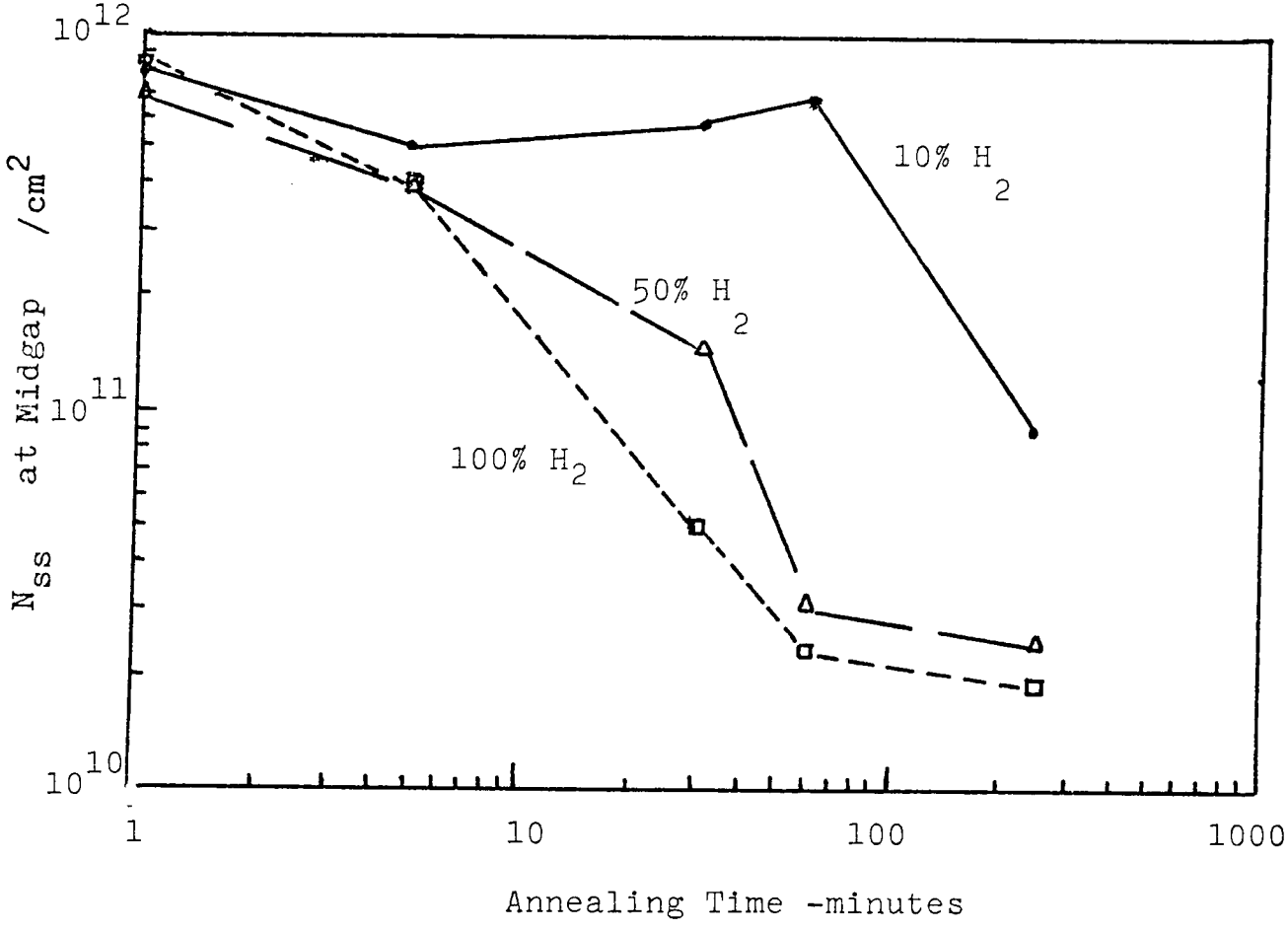


Figure 7. N_{ss} Versus Time - 400°C

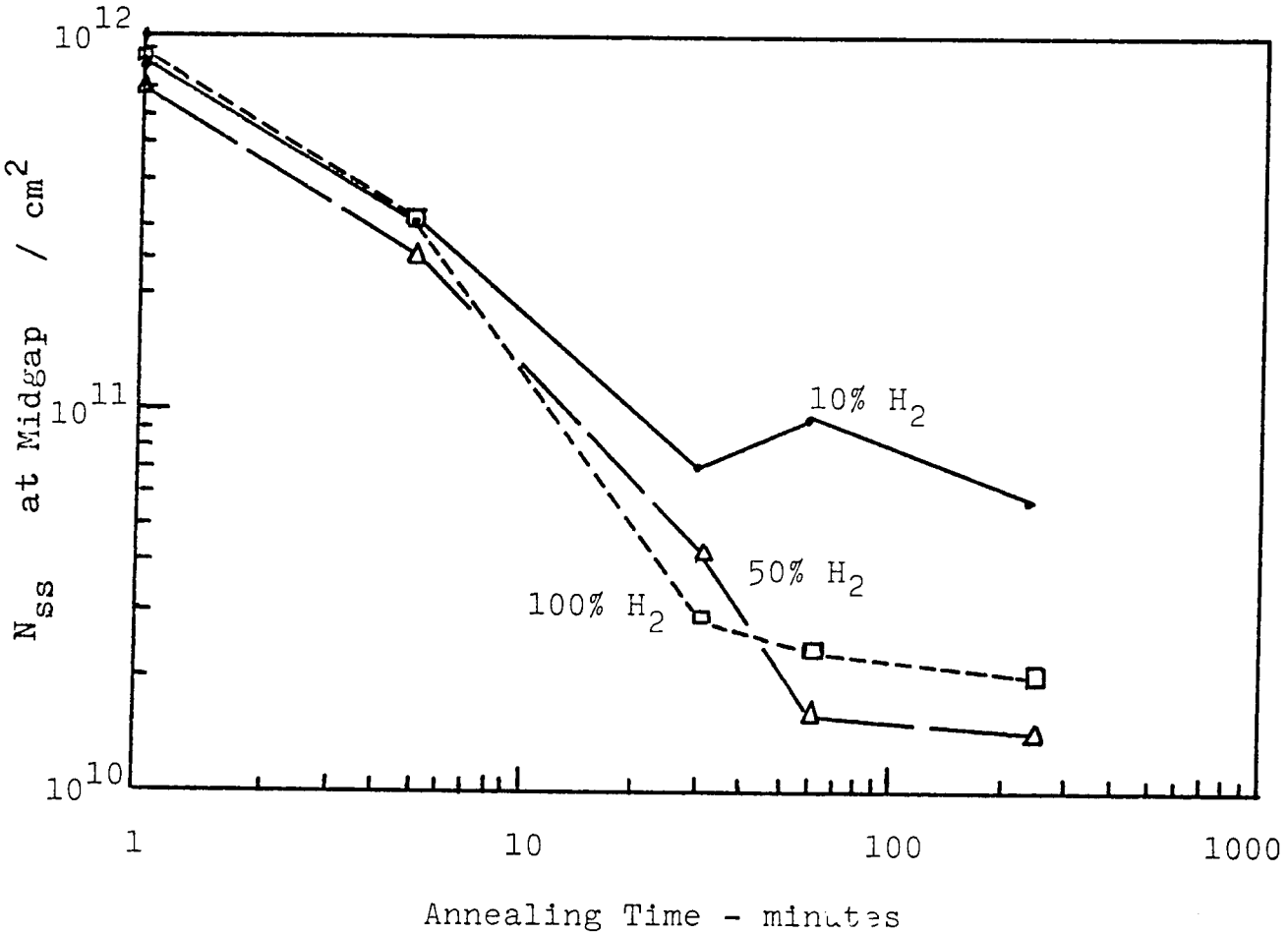


Figure 8. N_{ss} Versus Time - 500°C

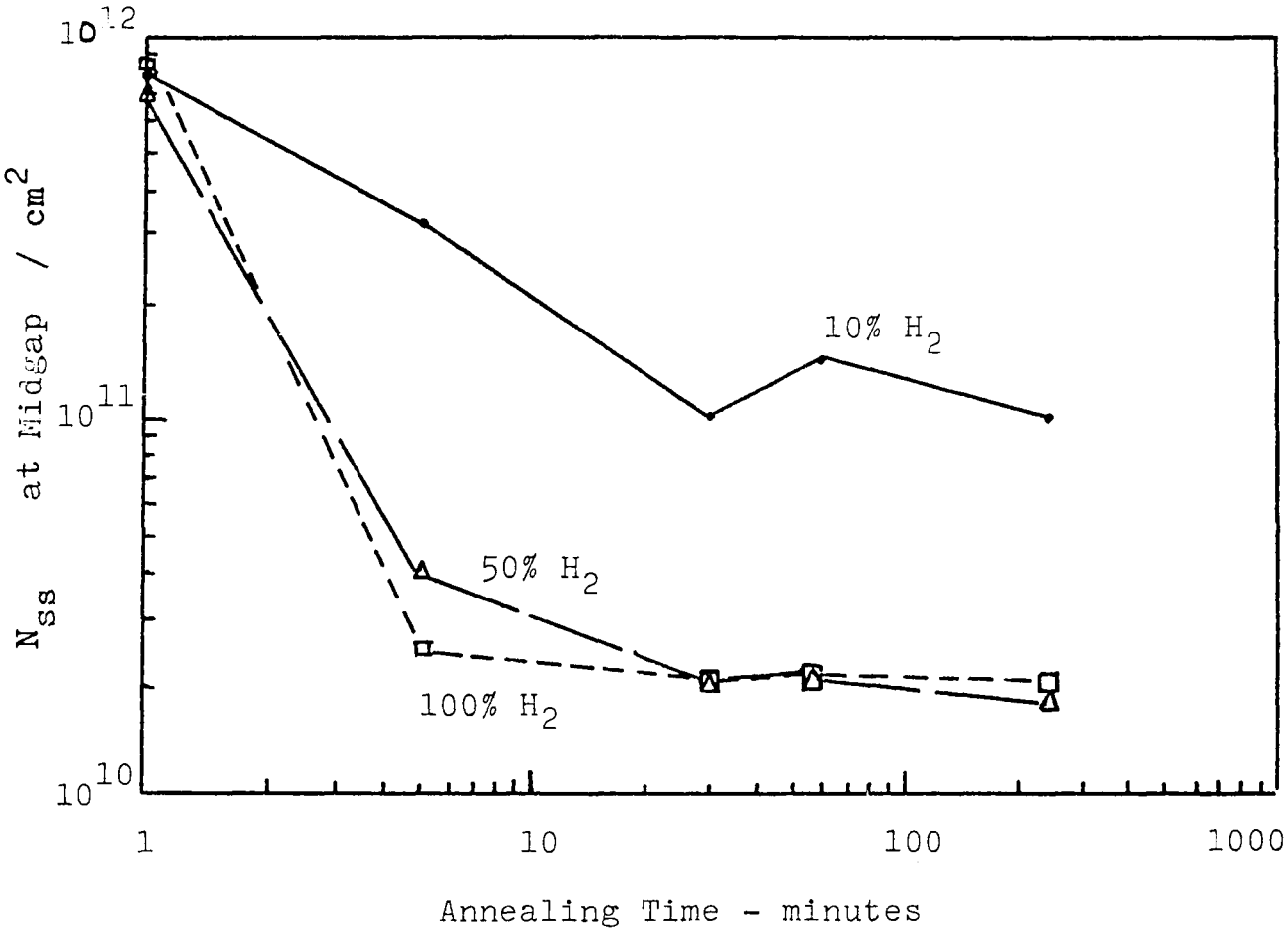


Figure 9. N_{ss} Versus Time - 600°C

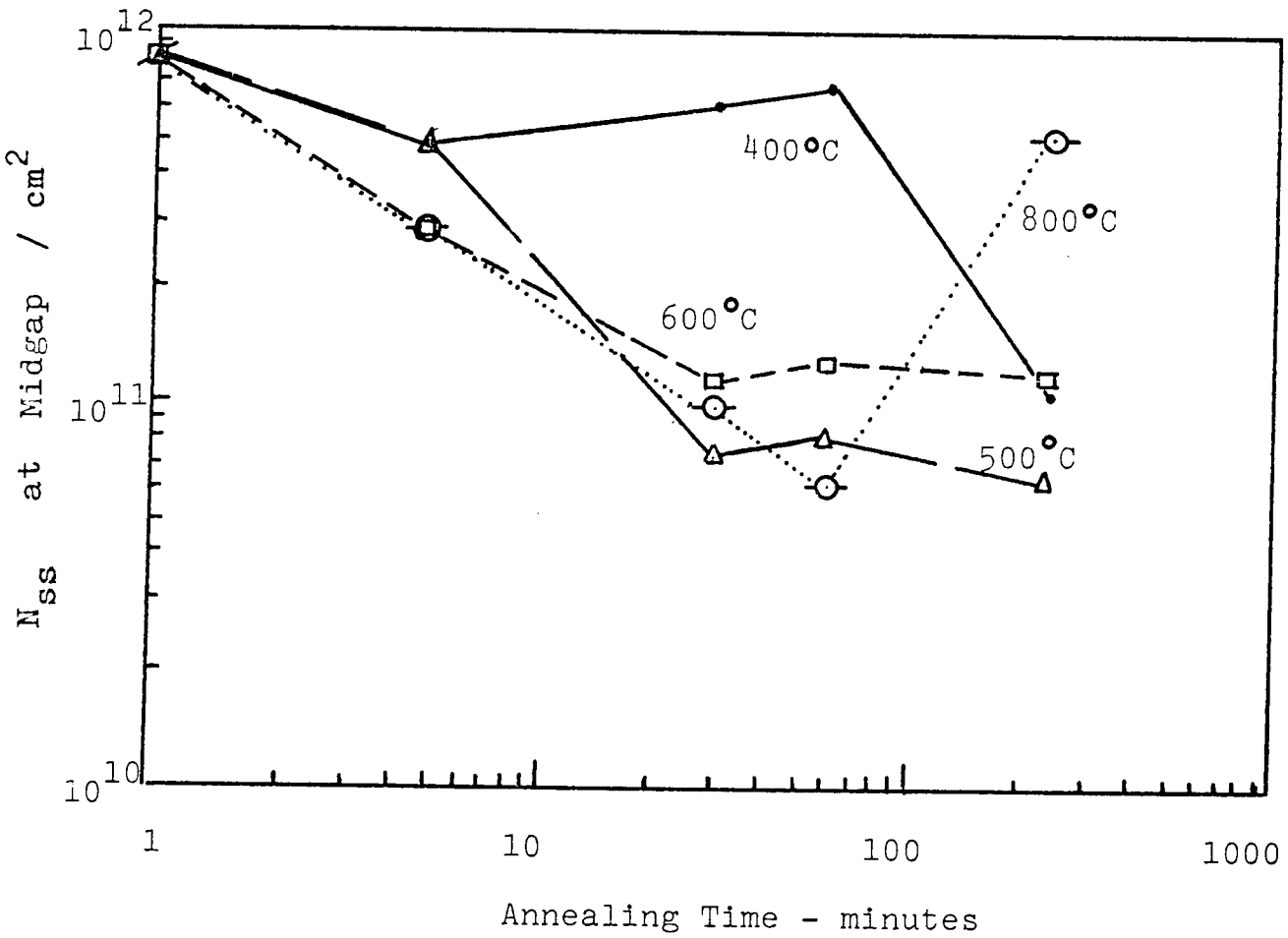


Figure 10. N_{ss} Versus Time - 10% H_2

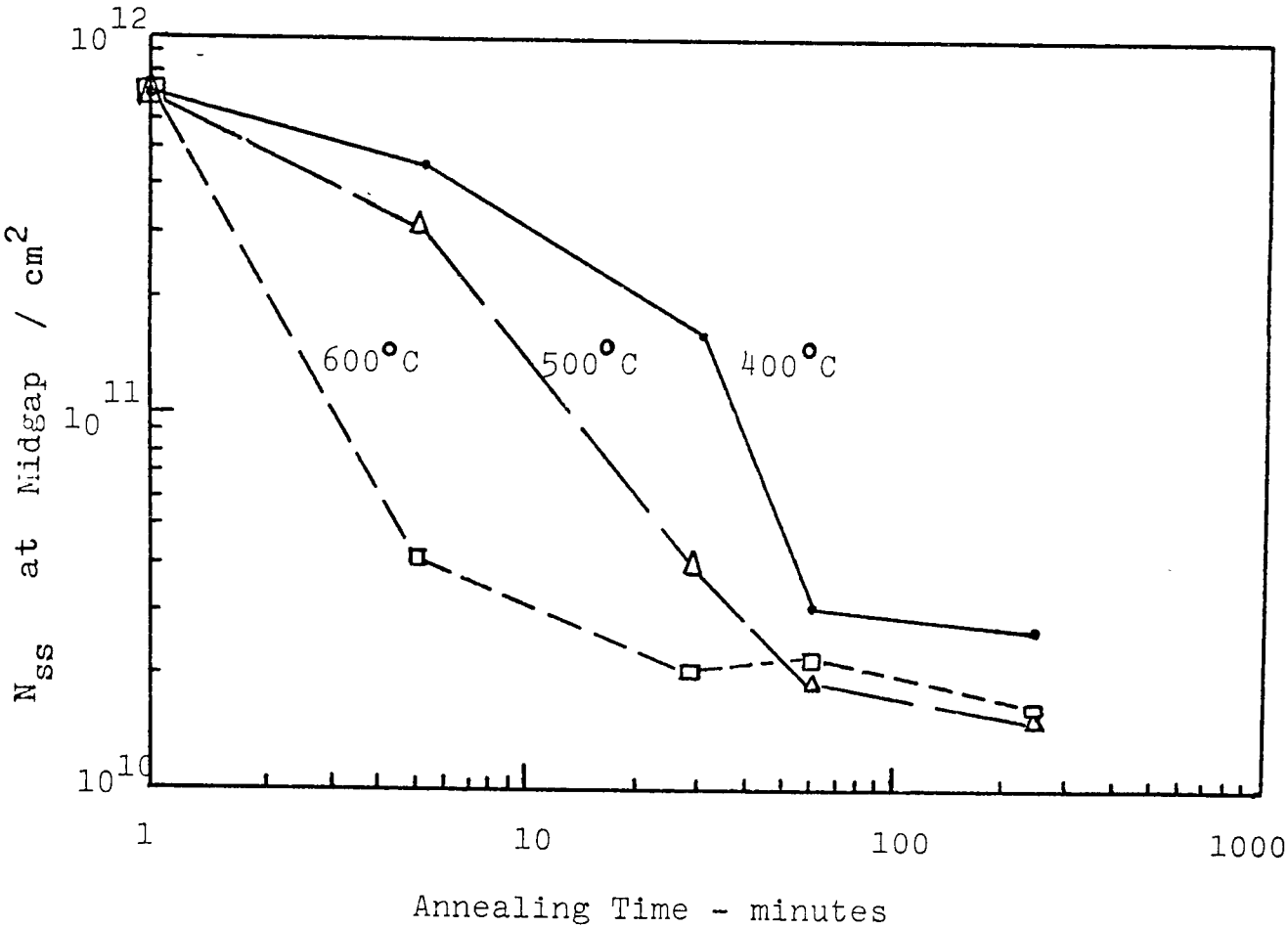


Figure 11. N_{ss} Versus Time - 50% H_2

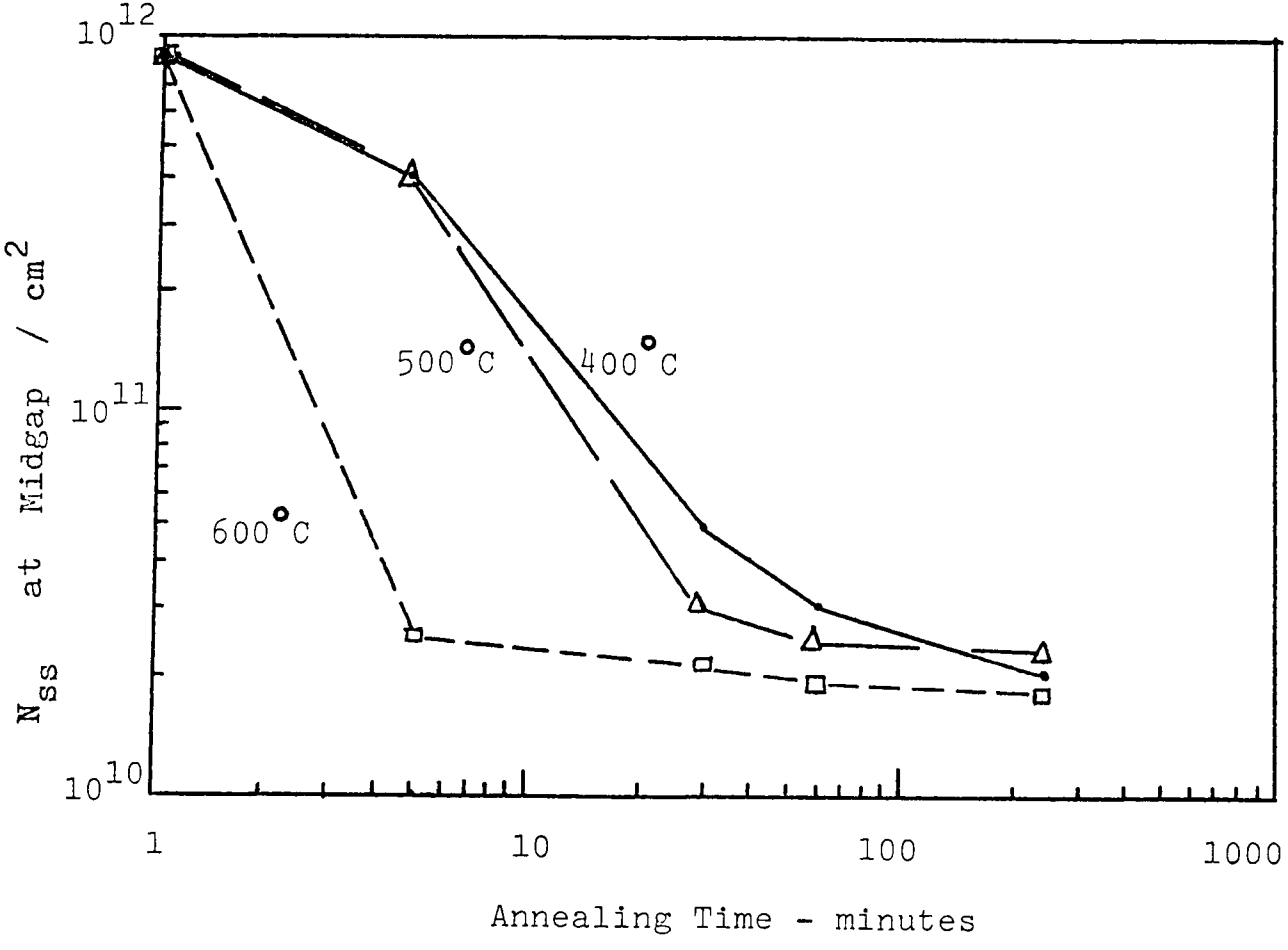


Figure 12. N_{ss} Versus Time - 100% H_2

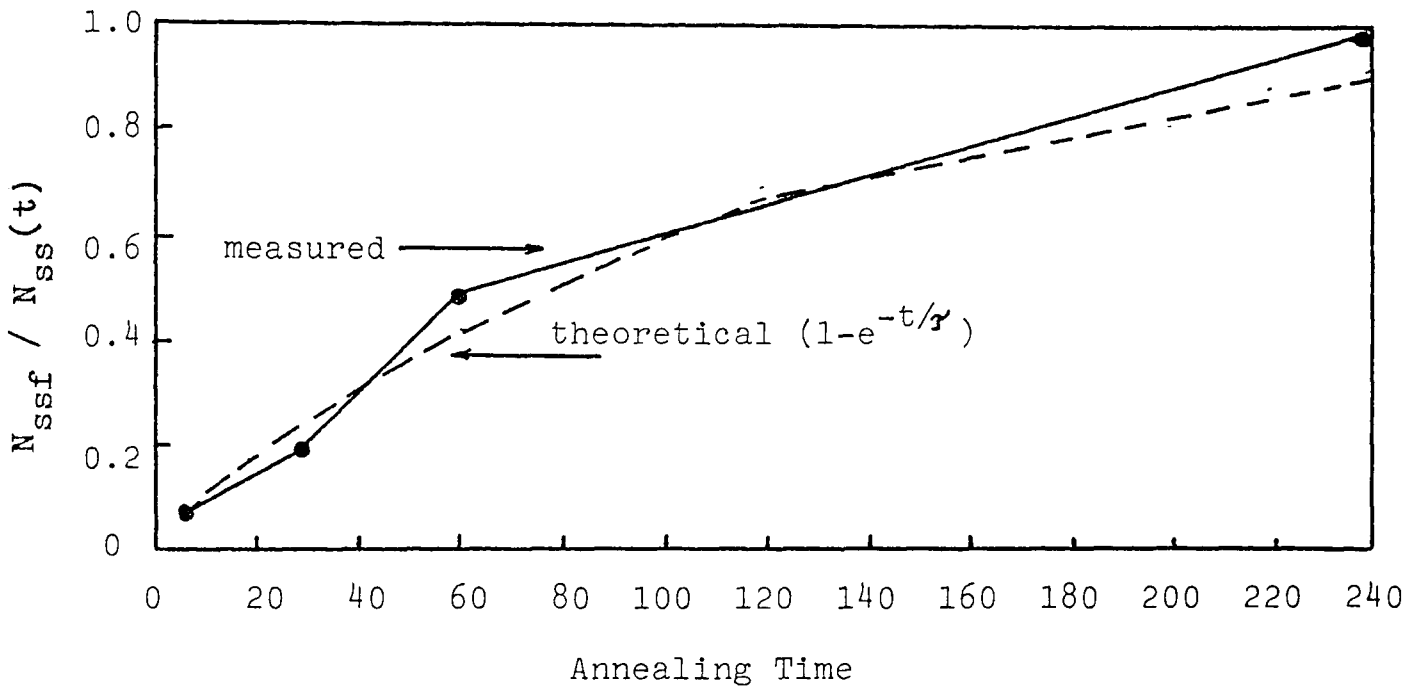
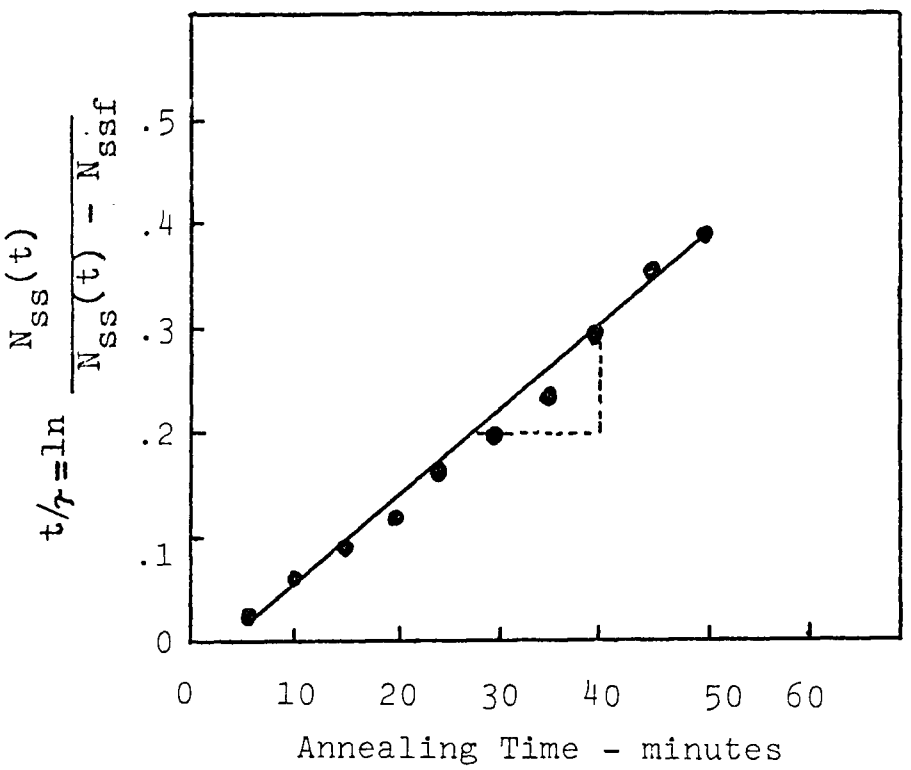


Figure 13. N_{ssf} / $N_{ss}(t)$ Versus Time - 400°C , 50% H_2



$$\text{slope} = \frac{.08}{10} = .008 = 1/\tau$$

Figure 14. t/τ Versus Time - 400°C, 50% H_2

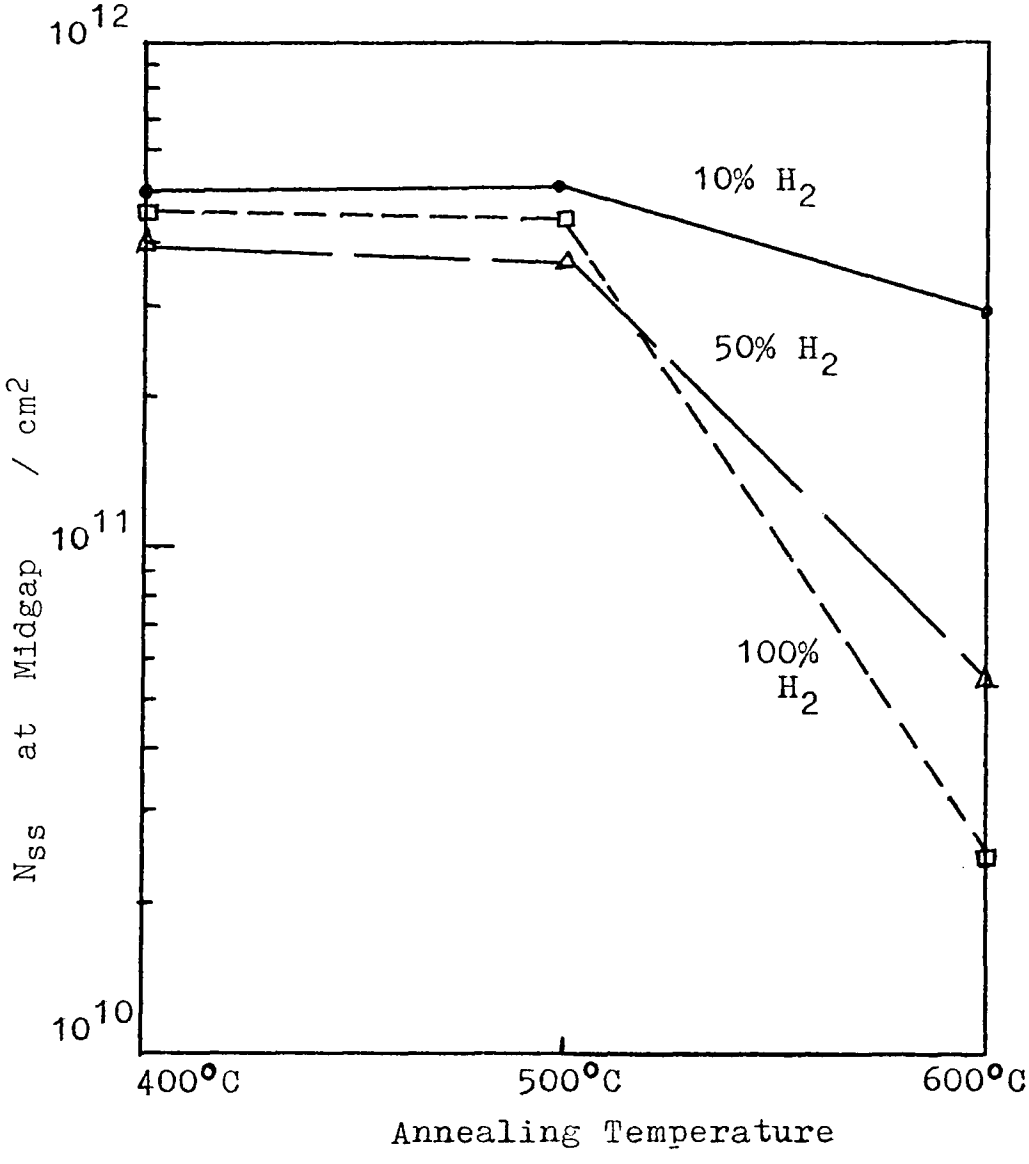


Figure 15. N_{ss} Versus Temperature - 5 min.

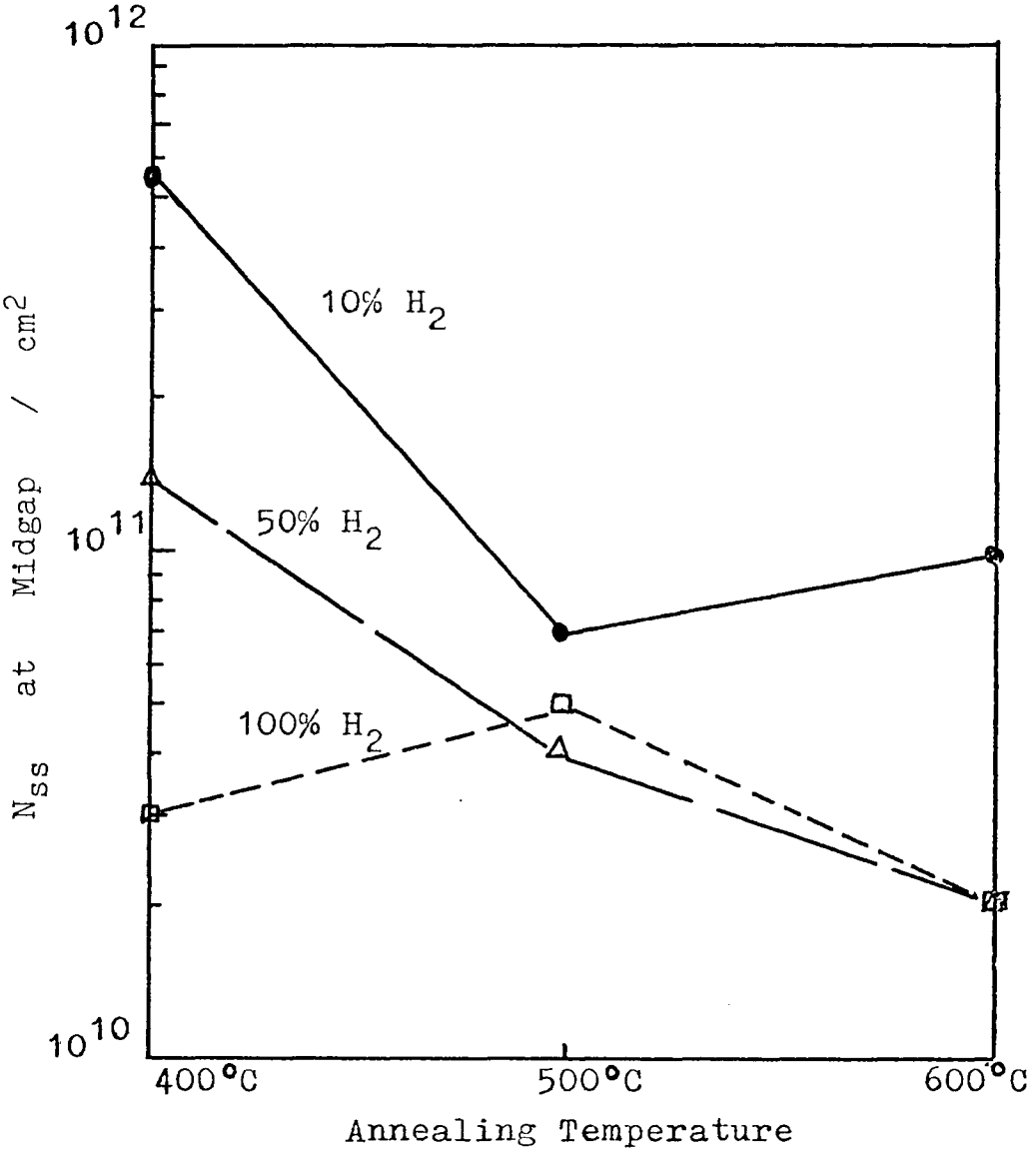


Figure 16. N_{ss} Versus Temperature - 30 min.

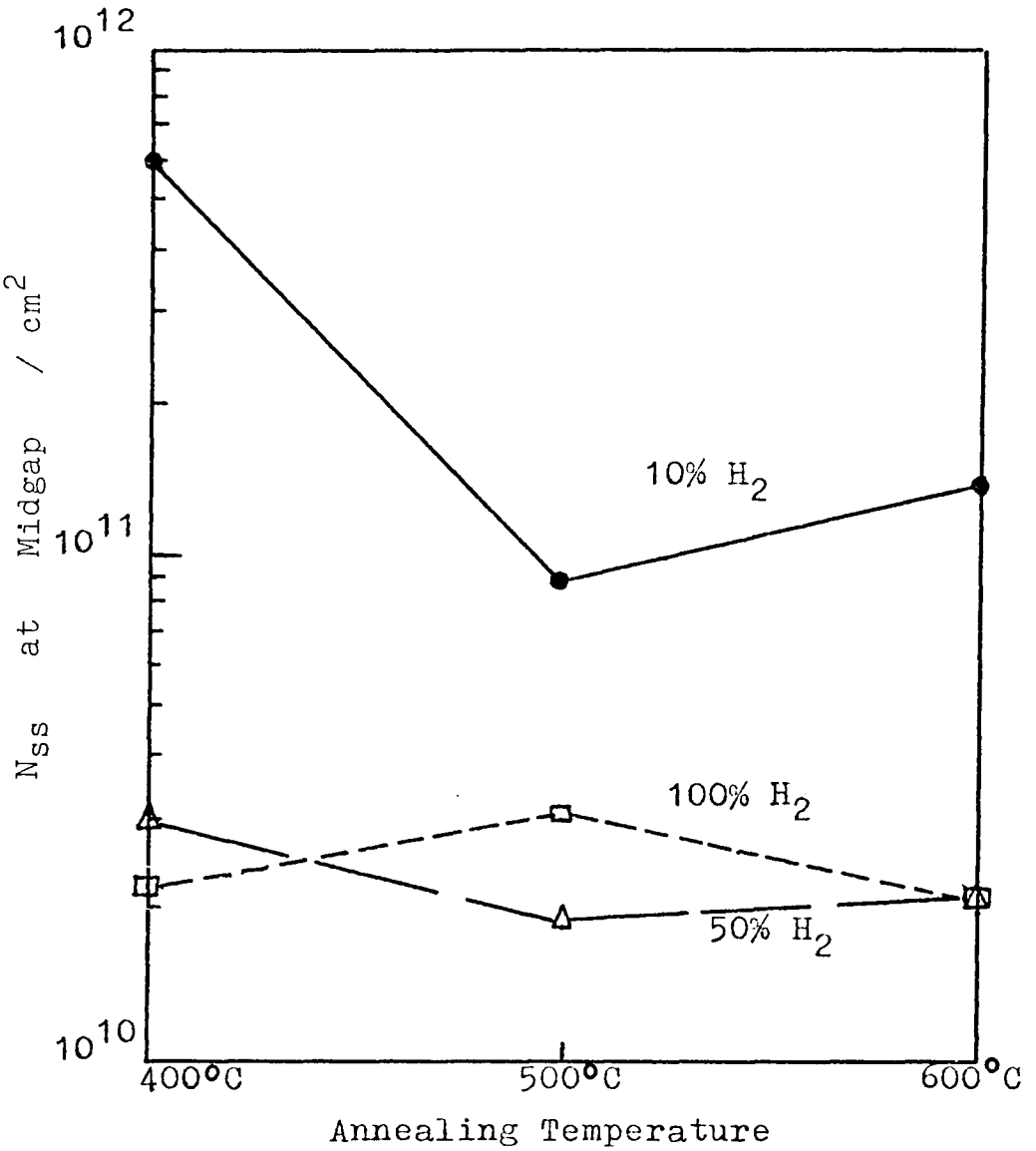


Figure 17. N_{ss} Versus Temperature - 60 min.

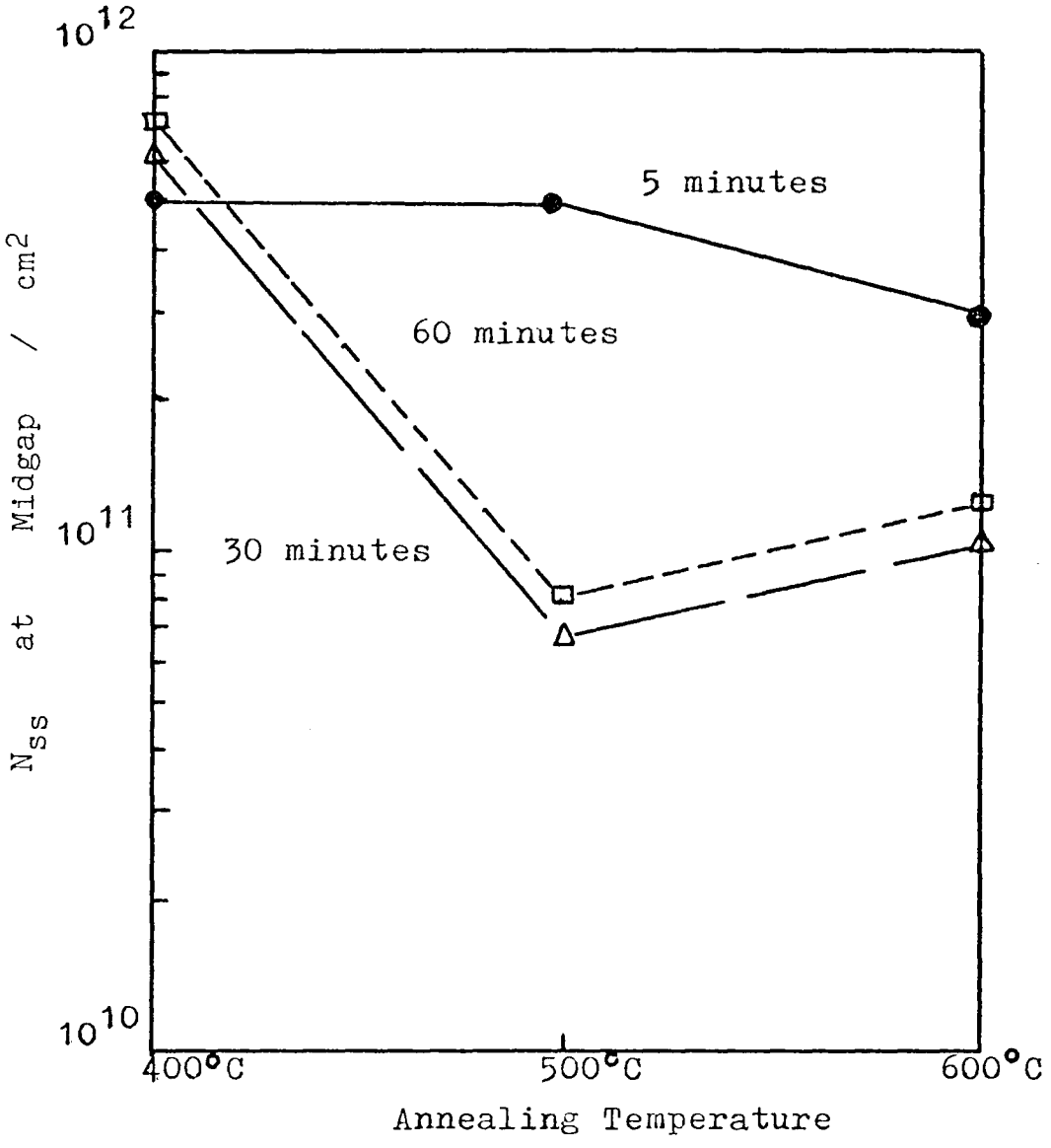


Figure 18. N_{ss} Versus Temperature - 10% H_2

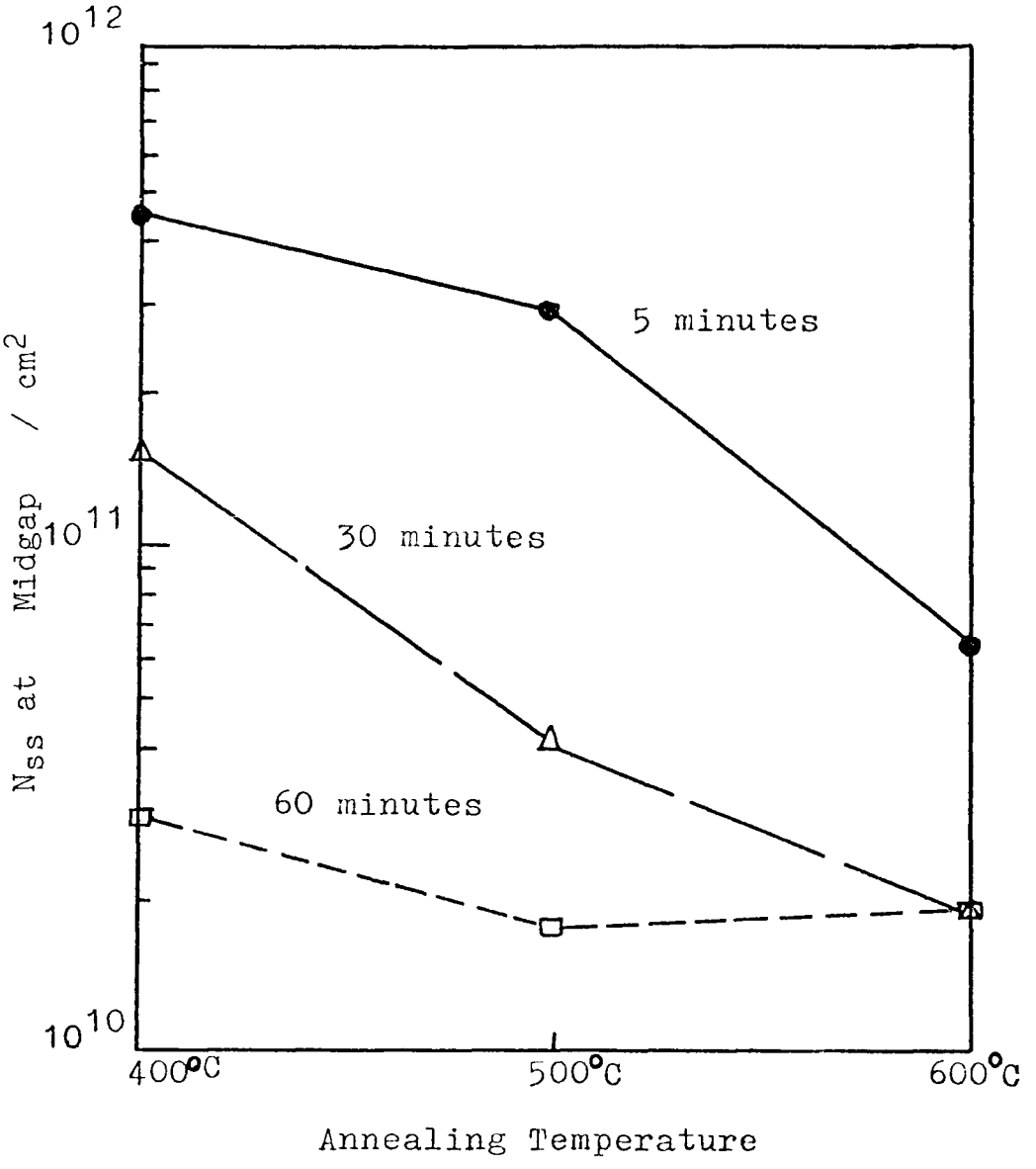


Figure 19. N_{ss} Versus Temperature-50% H_2

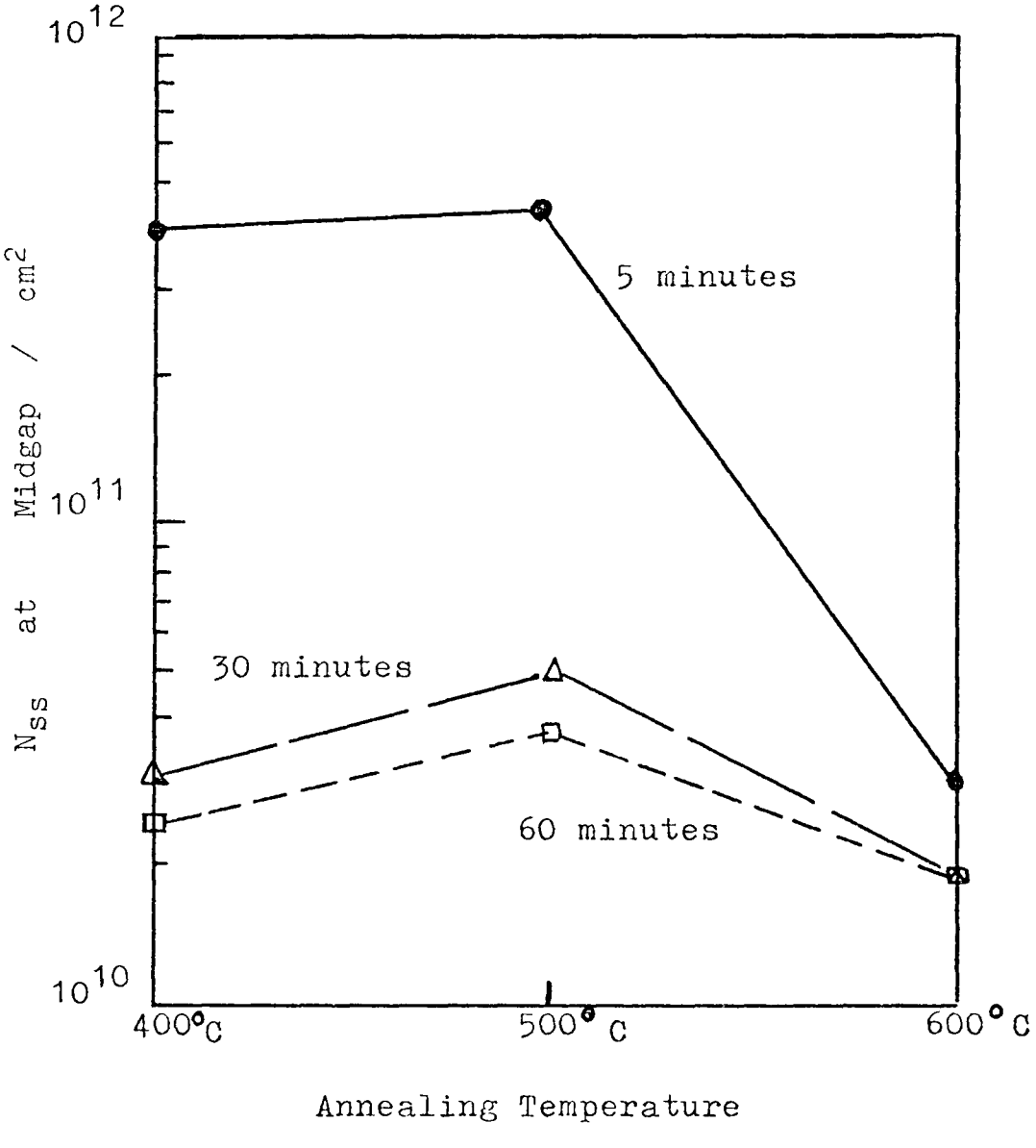


Figure 20. N_{ss} Versus Temperature-100% H_2

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BIOGRAPHICAL SKETCH

BRUCE WAYNE NONNEMAKER - Born March 24, 1947 in Allentown Pennsylvania. Parents names - Dorothy Elizabeth (Krauss) and Norman Norwood Nonnemaker, Married Barbara Louise (Dreisbach), August 9, 1969. Two children: Daniel Paul 4, Stephen Andrew 2.

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EXPERIENCE - Employed by Western Electric Co. from June 1969 to present.

Assignments have included:

SAFEGUARD PROJECT - product engineer bipolar discrete transistors and integrated circuits

MOS - development engineer on MOS memory circuits

- product engineer for photolithographic pattern generation

MEMBER - Phi Eta Sigma
Eta Kappa Nu
Sigma Tau
Tau Beta Pi